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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,413	02/27/2004	Yukihiro Urakawa	249344US2SDIV	4542
22850	7590	02/26/2008	EXAMINER	
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314				QUINTO, KEVIN V
ART UNIT		PAPER NUMBER		
		2826		
NOTIFICATION DATE			DELIVERY MODE	
02/26/2008			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/787,413	URAKAWA, YUKIHIRO	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 28 November 2007.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-3,5,6 and 8-20 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 1-3,5,6,8 and 16 is/are allowed.
 6) Claim(s) 9,10,12-14,17 and 18 is/are rejected.
 7) Claim(s) 11,15,19 and 20 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____. | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 9-15 and 17-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9, 10, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida (JP 4-364063 A).
4. In reference to claims 9, 17, and 18, Yoshida (JP 4-364063 A) discloses a structure which meets the claim. Figures 1 and 2 of Yoshida disclose an SiP (system in package) device comprising a chip on chip (COC) device having a logic chip (105) having a logic circuit and a memory chip (101) mounted on the logic chip (105). The memory chip (101) comprises basic chips (104) functioning as a chip independently from each other. A dicing line is interposed between the basic chips (104), connects the basic chips (104), and configures a part of the memory chip (101). A bump (106) connects the logic chip (105) and the memory chip (101). Although not shown, it is understood that a package covers the COC device. The logic chip (105) supplies

signals to the memory chip (101) since the logic chip is the CPU. With regard to the limitations in claims 9 and 18 concerning the control signal changing the specification of the basic chip, a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. Therefore these limitations do not render the claims patentable over Yoshida.

5. With regard to claim 10, it is understood that the basic chips (104) have the same layout.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (JP 4-364063 A) in view of Tsuji et al. (USPN 5,716,889) and further in view of Natsume et al. (USPN 5,477,062) and further in view of Dasse et al. (USPN 5,399,505).

8. In reference to claim 12, Yoshida does not disclose the use of an alignment mark in the dicing line. However the use of an alignment mark in the dicing line is well known in the art. Tsuji et al. (USPN 5,716,889, hereinafter referred to as the "Tsuji" reference) discloses that alignment marks in the dicing line provide alignment which is important

for precise fine patterning (column 1, lines 15-39), and that precise alignment is a known goal in the art (column 1, lines 40-42). In view of Tsuji, it would therefore be obvious to provide an alignment mark in the dicing line. Yoshida does not disclose the use of a test element group in the dicing or scribing line. However the use of a test element group in the dicing or scribing line is well known in the art. Natsume et al. (USPN 5,477,062, hereinafter referred to as the “Natsume” reference) discloses that test element groups in the dicing or scribing line allow for performance testing of basic elements (column 1, lines 13-19). Dasse et al. (USPN 5,399,505, hereinafter referred to as the “Dasse” reference) discloses that testing is needed in order to determine whether or not a die is functional and that a known goal in the art is to detect and screen out defective circuitry as early as possible during the manufacturing process (column 1, lines 12-59). In view of Natsume and Dasse, it would therefore be obvious to provide a test element group in the dicing or scribing line.

9. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida (JP 4-364063 A).

10. With regard to claim 13, Yoshida teaches all of the claimed invention except for the square shape and exact length of the basic chip. Although Yoshida does not teach the exact square shape and length as that claimed by Applicant:

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416.

Therefore claim 13 is not patentably distinguishable over the Yoshida reference.

11. With regard to claim 14, Yoshida teaches all of the claimed invention except for the width of the dicing line. Although Yoshida does not teach the exact width as that claimed by Applicant:

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416.

Therefore claim 14 is not patentably distinguishable over the Yoshida reference.

Allowable Subject Matter

12. Claims 1-3, 5, 6, 8, and 16 are allowed.

13. Claims 11, 15, 19, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests or renders obvious a chip on chip device formed of a memory chip connected to a logic chip by a bump such that the memory chip contains basic chips (mounted by bumps) which are connected by a dicing line which has an alignment mark and a test element group as suggested in

claim 1. The examiner is also unaware of any prior art which suggests or renders obvious a chip on chip device formed of a memory chip connected to a logic chip by a bump such that the memory chip contains basic chips which are connected by a dicing line where the logic chip outputs a control signal to the memory chip in order to change a specification in each basic chip having the inverted basic chip layout as suggested in claim 11 and the basic chip bump connection as suggested in claim 15. The examiner is also unaware of any prior art which suggests or renders obvious a chip on chip device formed of a memory chip connected to a logic chip by a bump such that the memory chip contains basic chips which are connected by a dicing line where the logic chip outputs a control signal to the memory chip in order to change a specification in each basic chip while also having a specific type of memory chip mounted onto the logic chip in combination with the specific type of memory chip used for the basic chips as suggested in claims 19 and 20.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KVQ

*/A. Sefer/
Primary Examiner
Art Unit 2826*